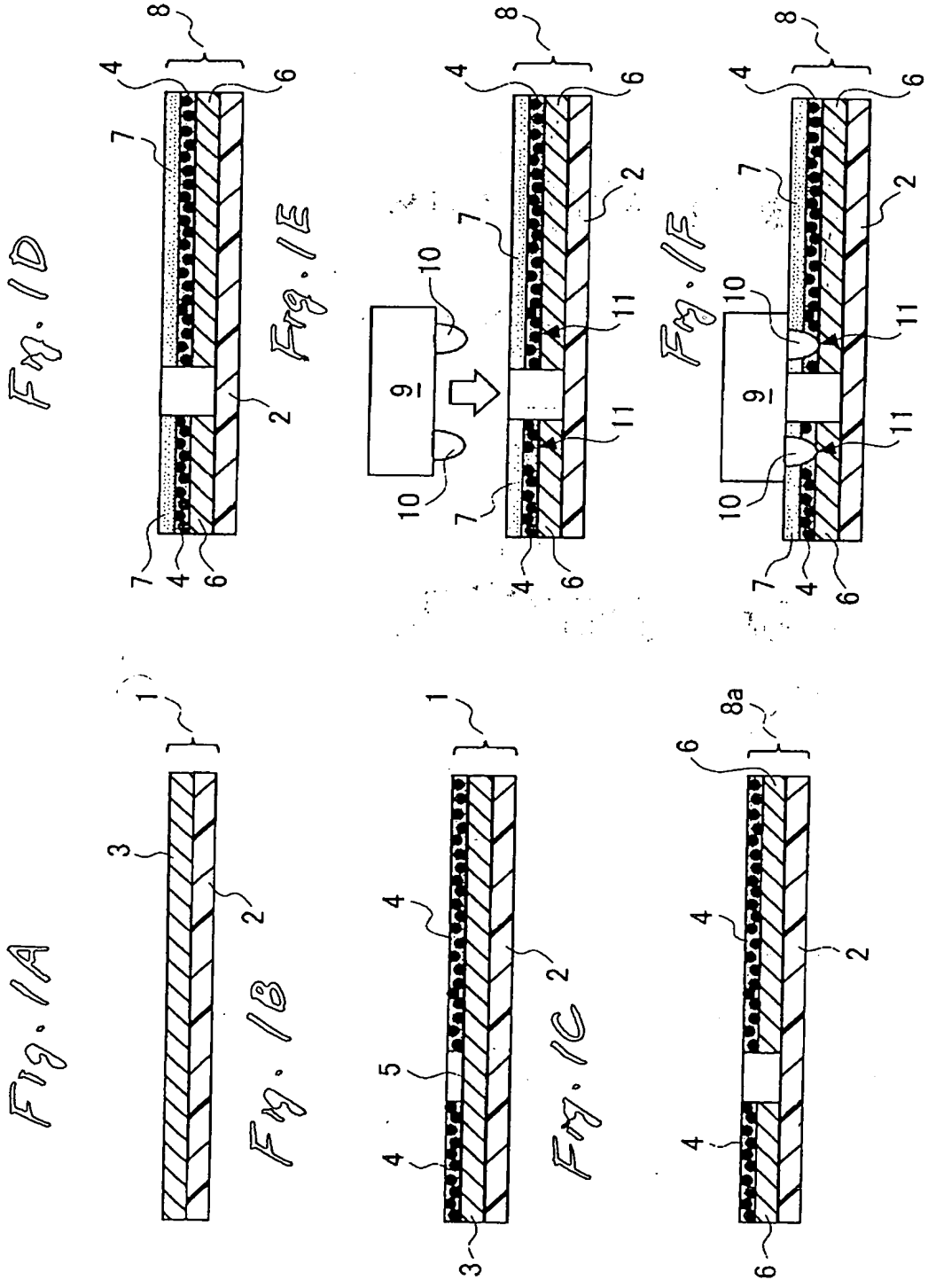


Fig. 1A
Fig. 1B
Fig. 1C
Fig. 1D
Fig. 1E
Fig. 1F

Fig. 2A

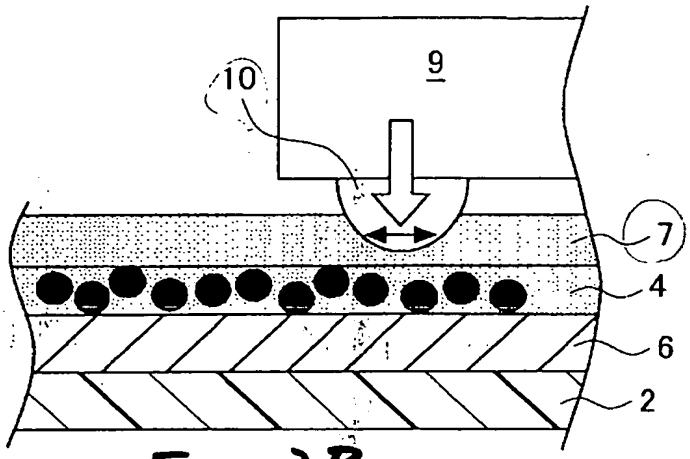


Fig. 2B

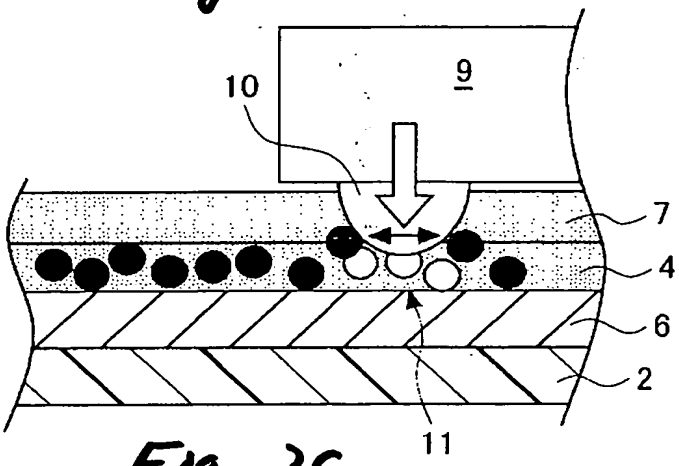


Fig. 2C

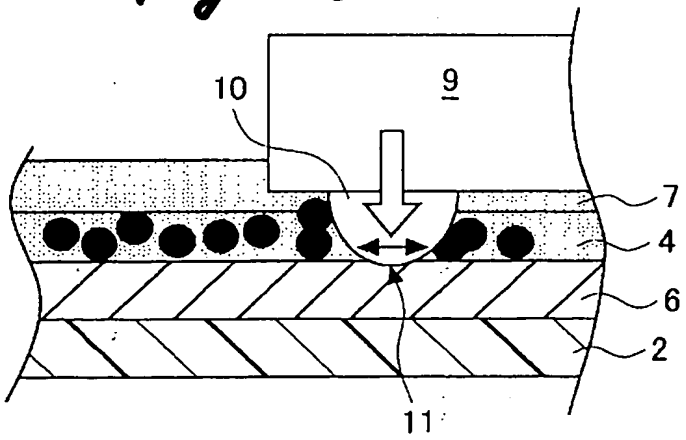


Fig. 3A

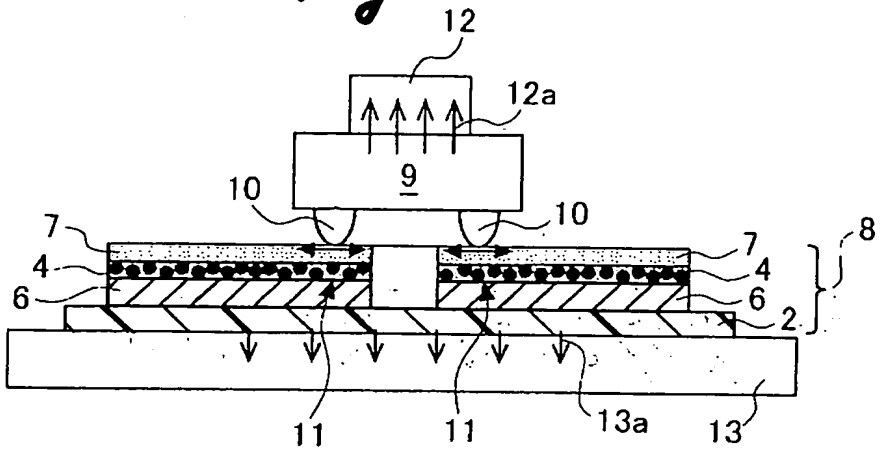


Fig. 3B

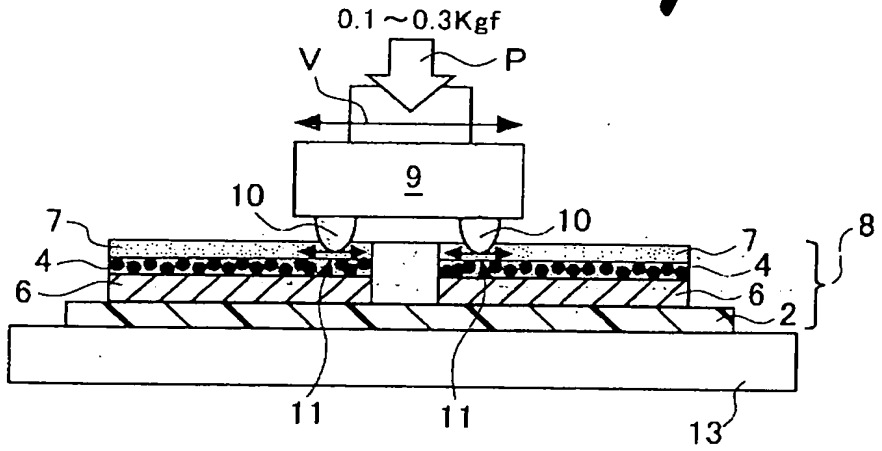


Fig. 3C

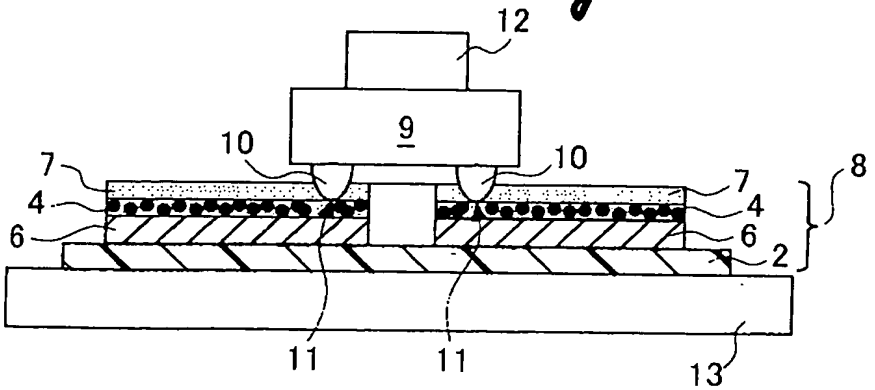


Fig. 4A

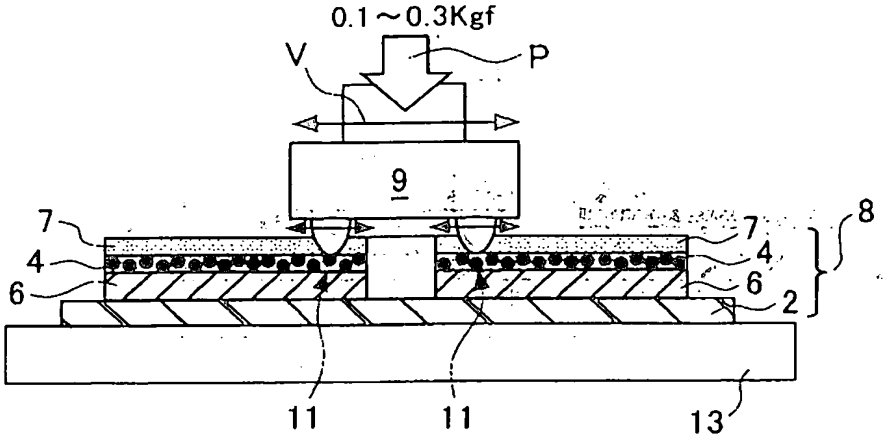


Fig. 4B

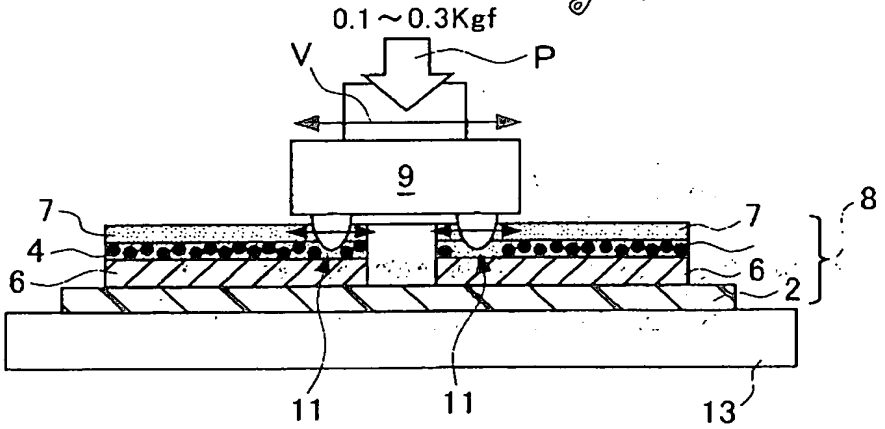


Fig. 4C

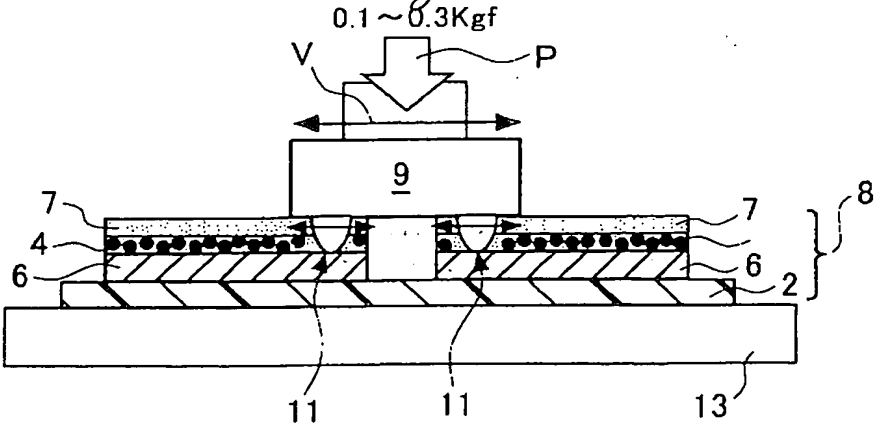


Fig. 5

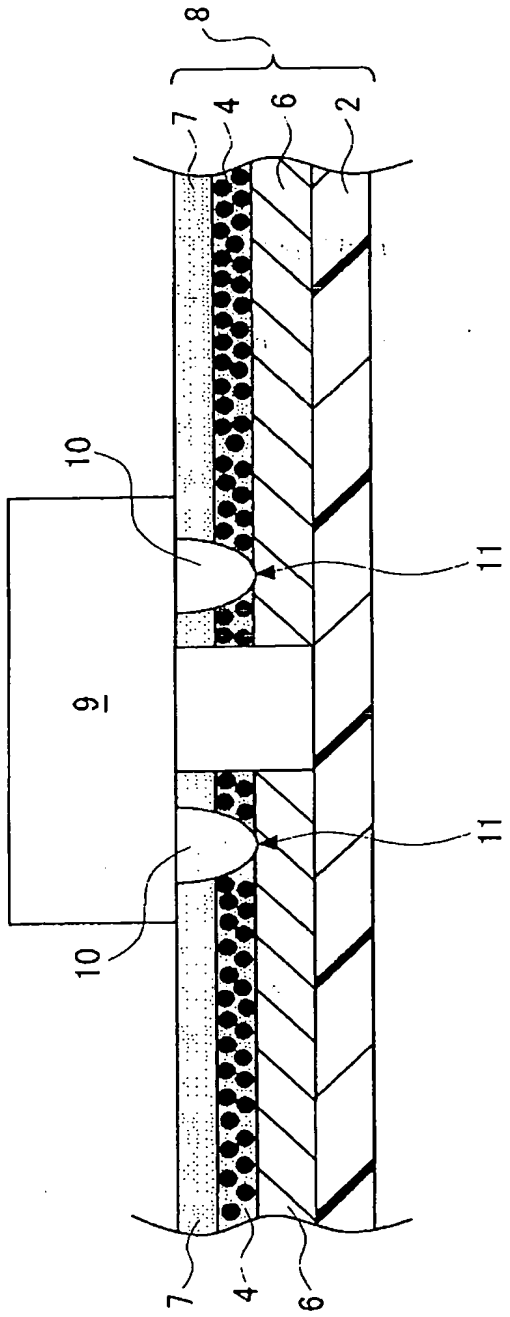


Fig. 6A

Semiconductor Mounting Method	Ultrasonic Bonding	Embodiment
Bonding Strength	200～250	1400～1700

Fig. 6B

Semiconductor Mounting Method	Third Method of the related art	Embodiment
Short-Circuit failure Occurrence Ratio	5.0%	0.0%

Fig. 7A

SiO_2 Particles	None	Present (Embodiment)
Semiconductor chip bonding failure (100 tests)	96.0%	0.0%

Fig. 7B

SiO_2 Particles	1~2 μm	3~4 μm (Embodiment)
Semiconductor chip bonding failure (100 tests)	50.0%	0.0%

Fig. 8

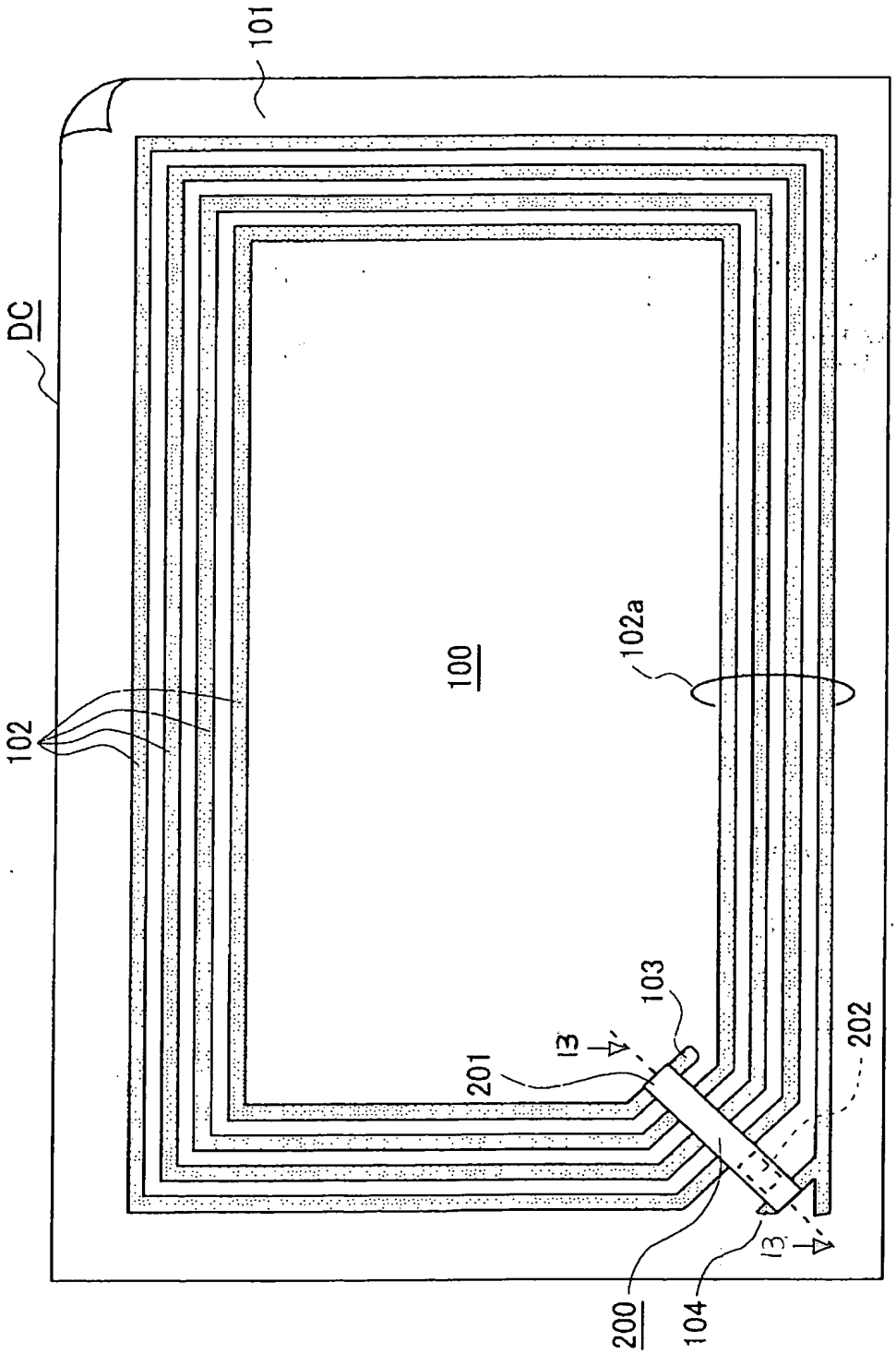


Fig. 9

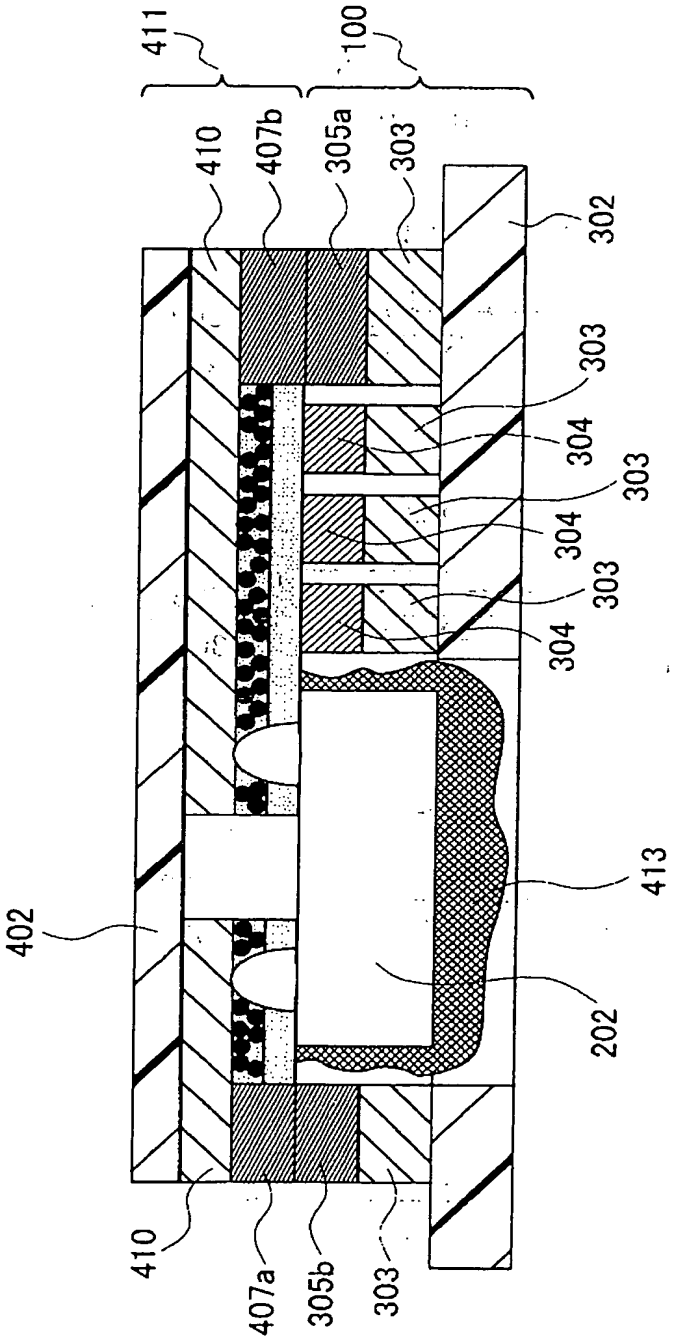

411
100
410
407b
305a
303
302
303
304
303
304
303
304
413
402
202
410
407a
305b
303

Fig. 10A

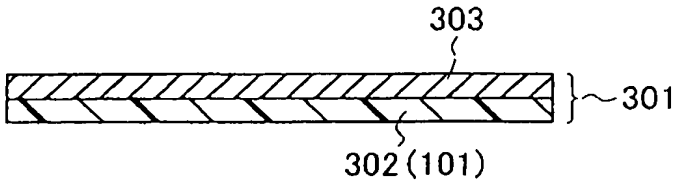


Fig. 10B

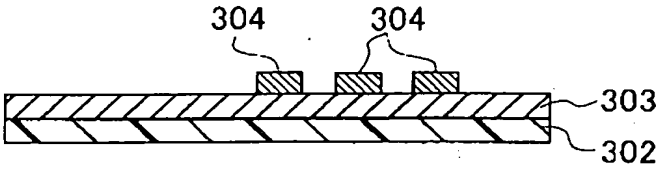


Fig. 10C

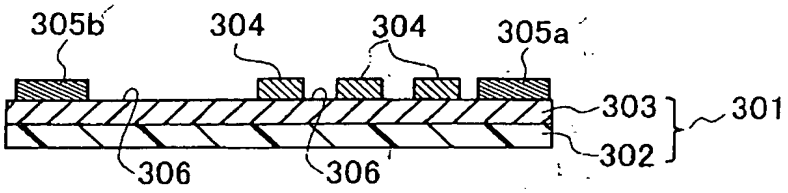


Fig. 10D

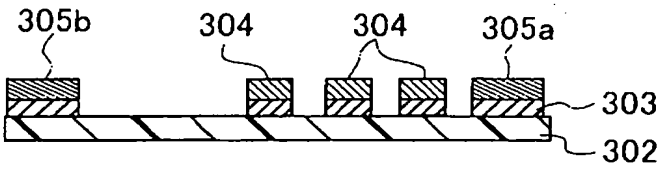
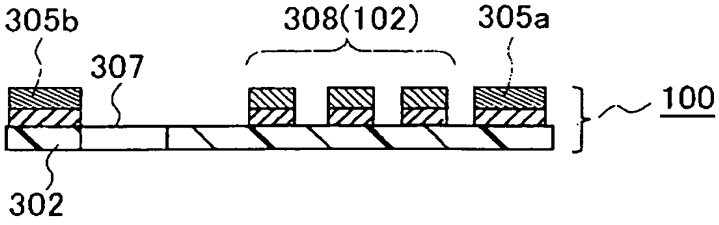


Fig. 10E



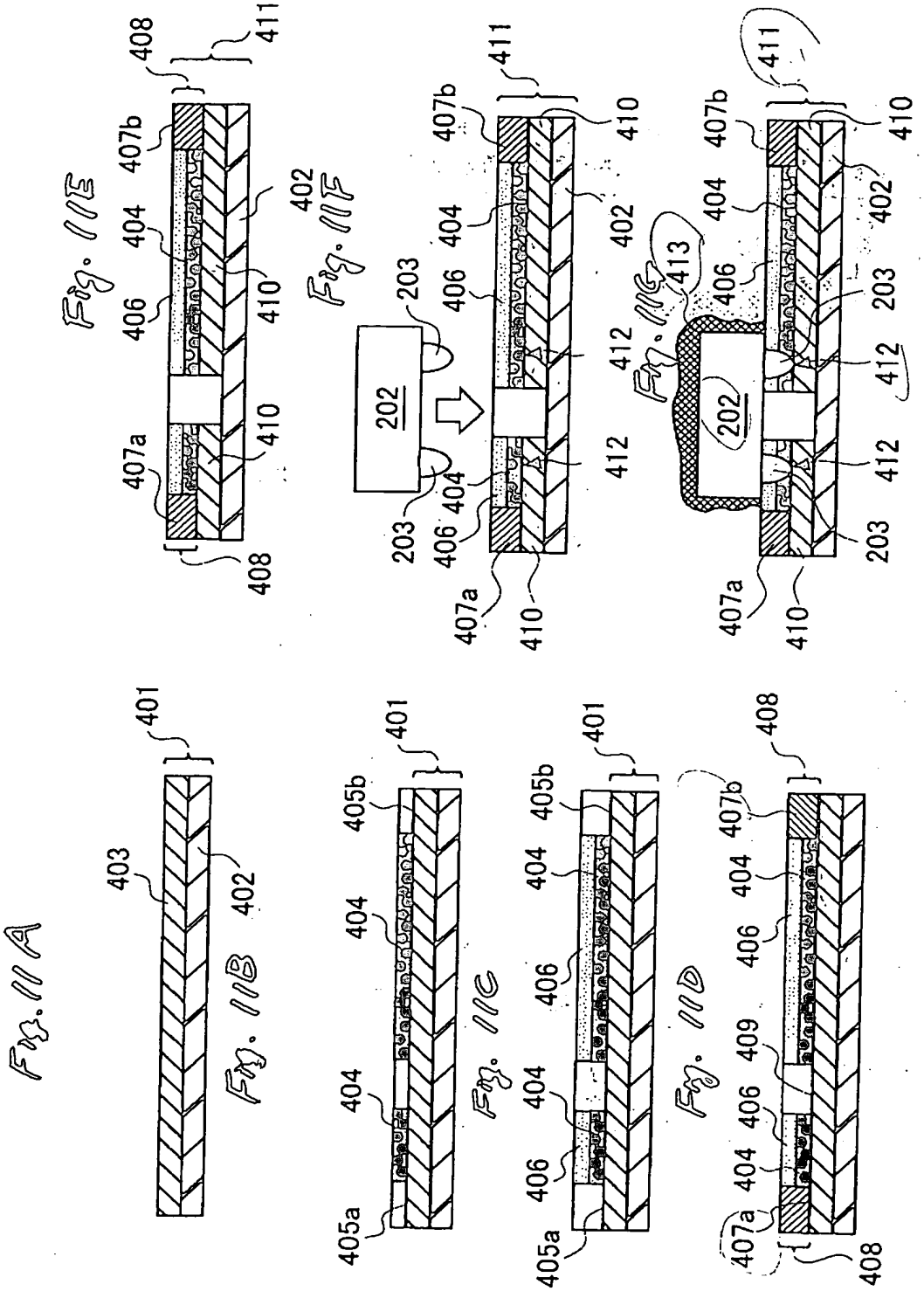


Fig. 11A
401
403
402
Fig. 11B
401
405b
404
405a
Fig. 11C
401
405b
404
406
405a
Fig. 11D
408
407b
404
406
409
407a
Fig. 11E
411
408
407b
404
406
410
407a
Fig. 11F
411
407b
410
402
404
406
203
202
412
203
406
404
407a
410
Fig. 11G
411
407b
410
402
404
413
406
203
412
202
412
203
407a
410

Fig. 12A

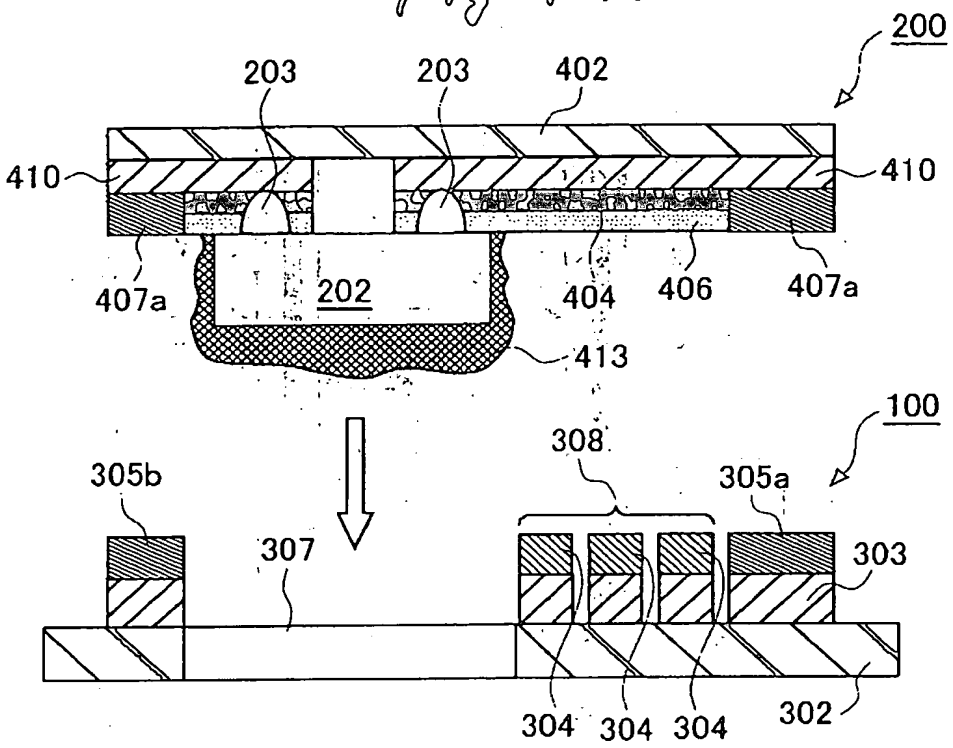


Fig. 12B

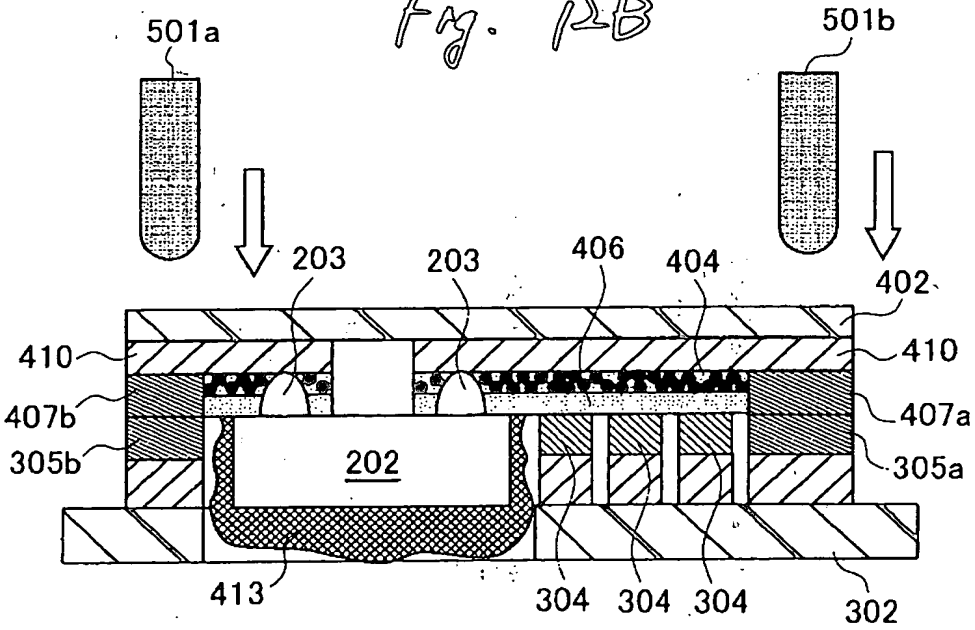


Fig. 13

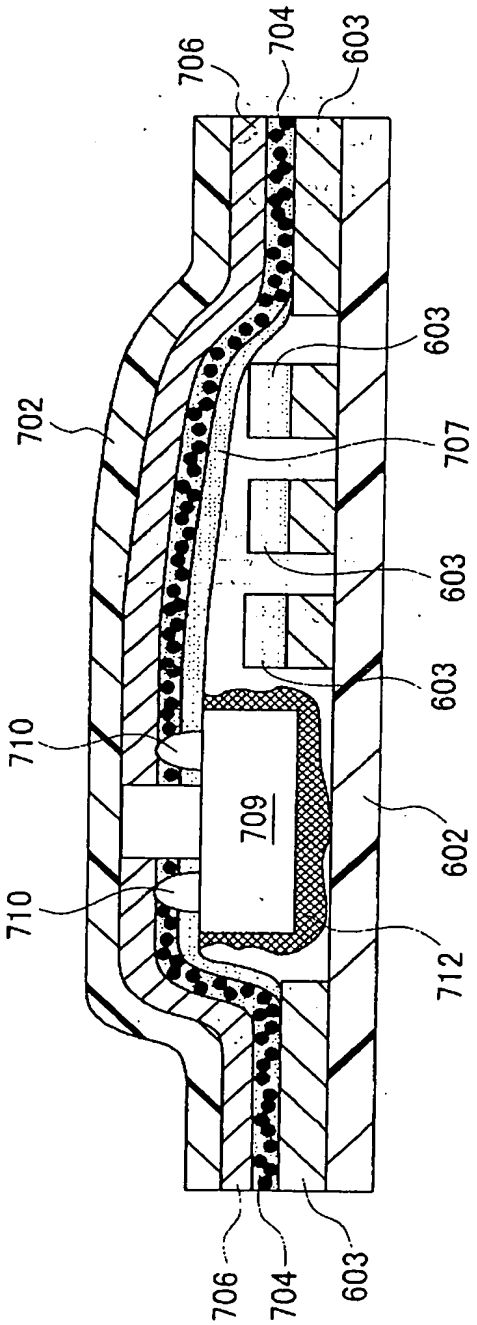


Fig. 14A

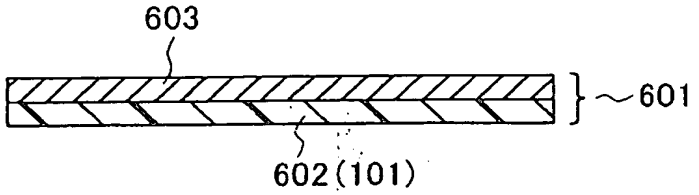


Fig. 14B

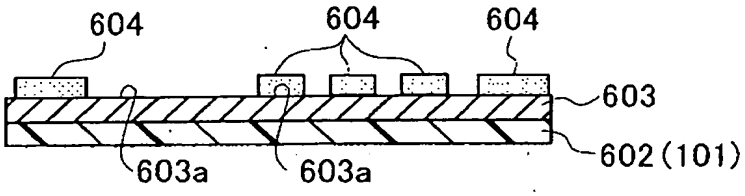


Fig. 14C

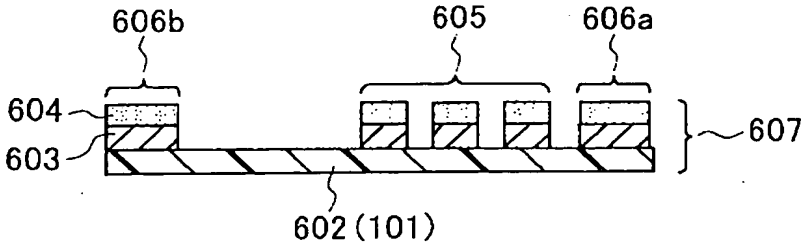


Fig. 1SA

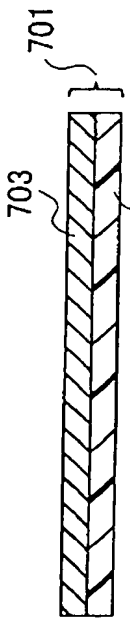


Fig. 1SB

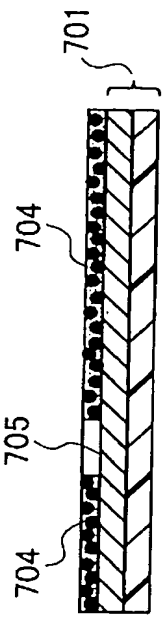


Fig. 1SC

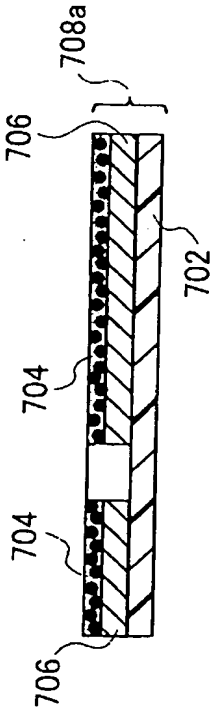


Fig. 1SD

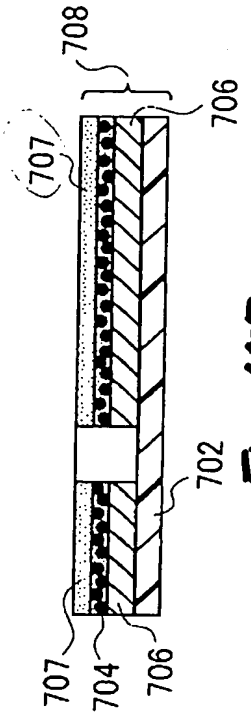


Fig. 1SE

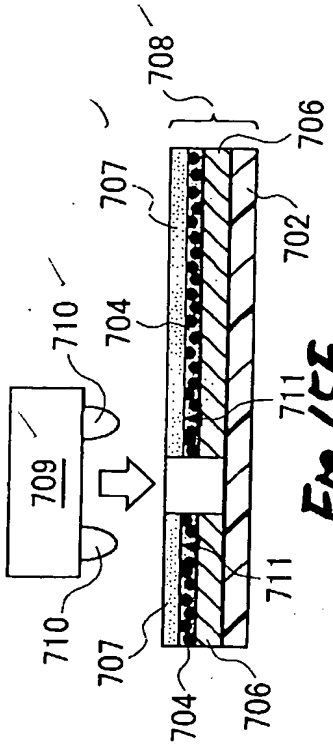


Fig. 1SF

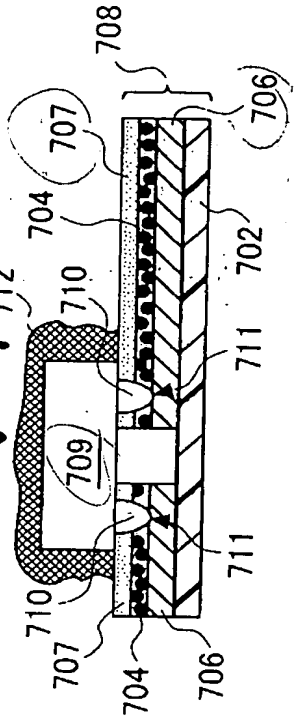


Fig. 16A

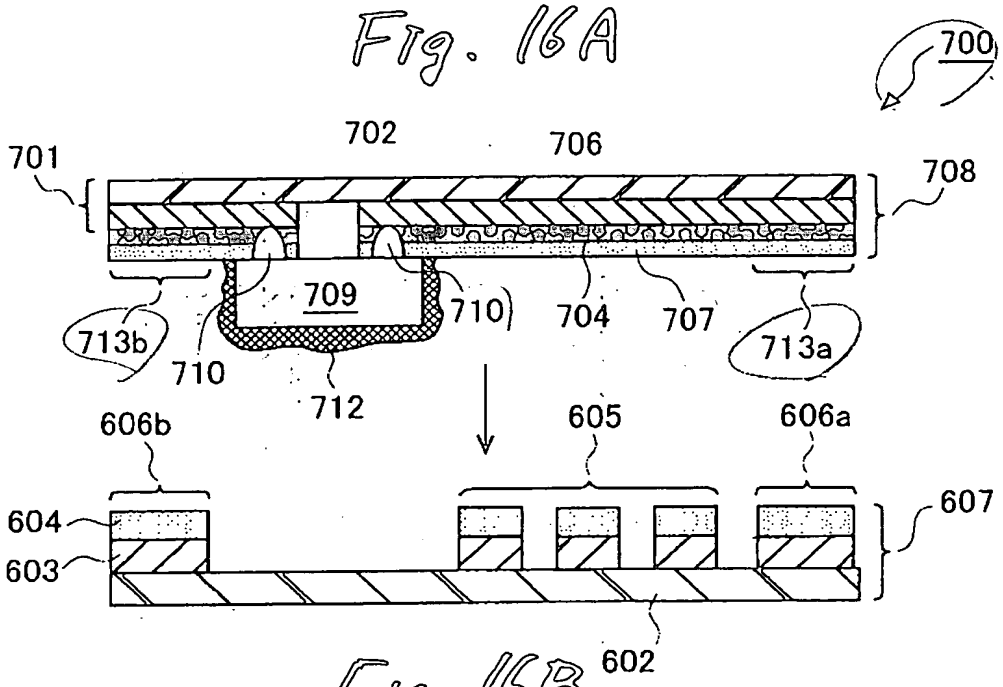


Fig. 16B

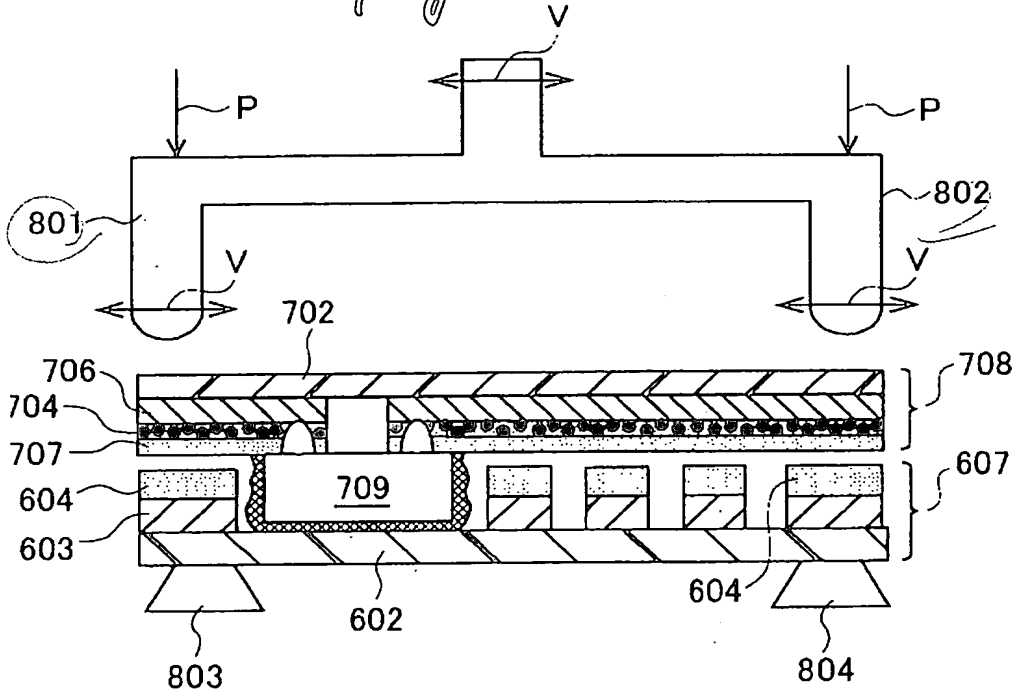


Fig. 17

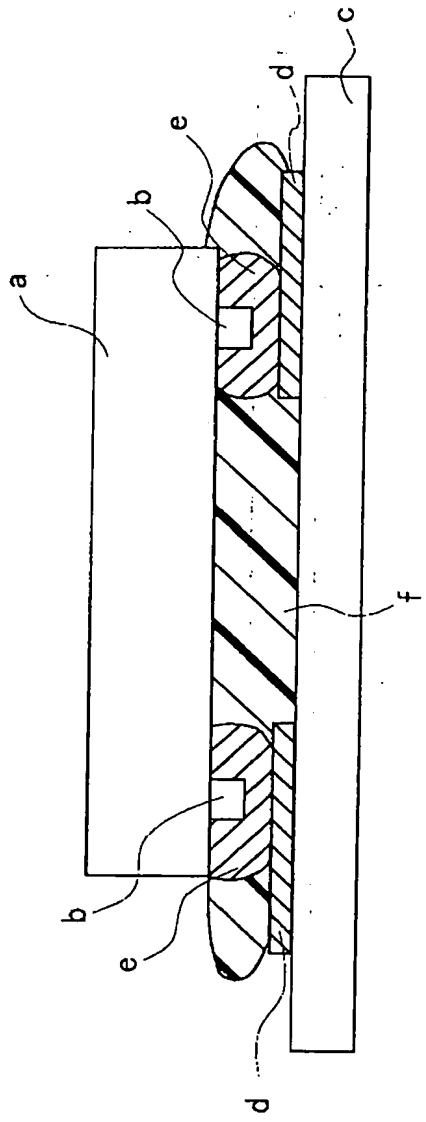


Fig. 18

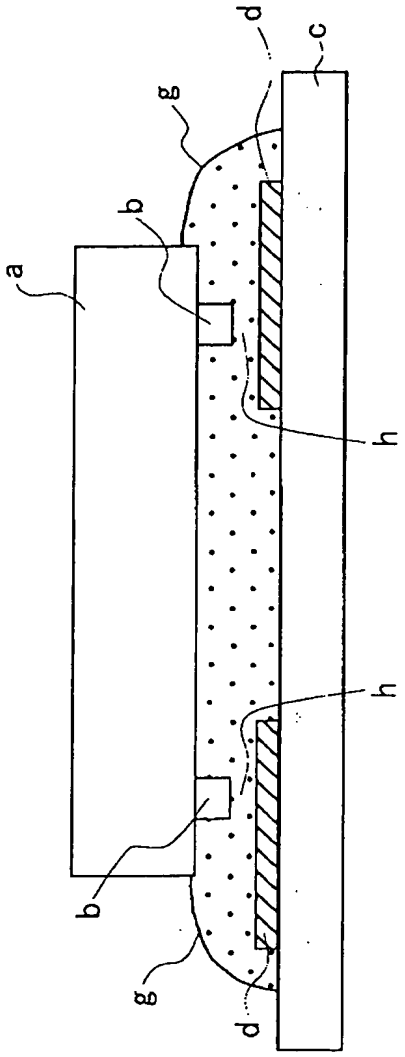


Fig. 19A

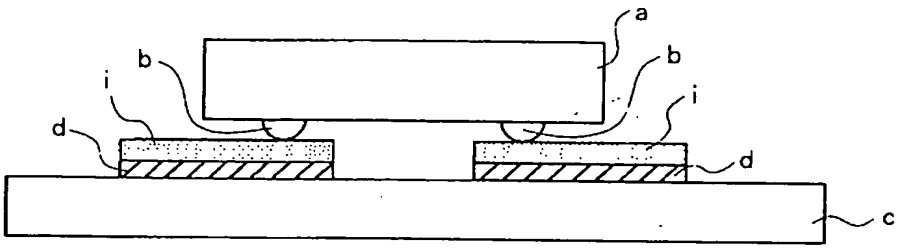


Fig. 19B

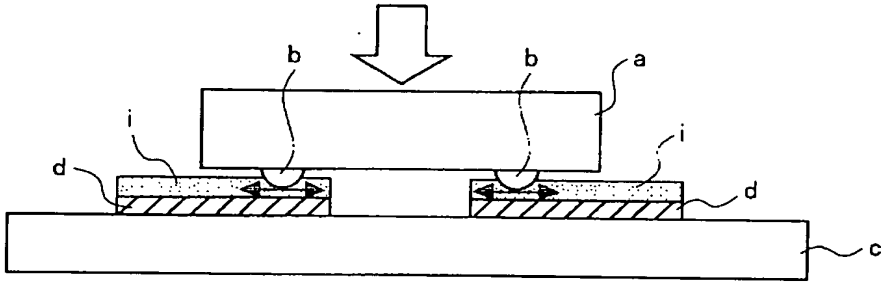


Fig. 19C

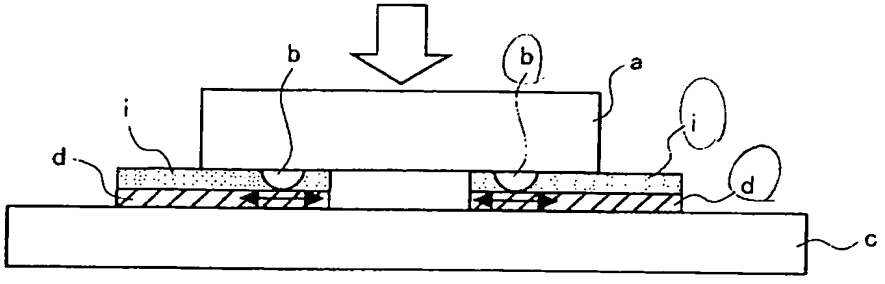


Fig. 20A

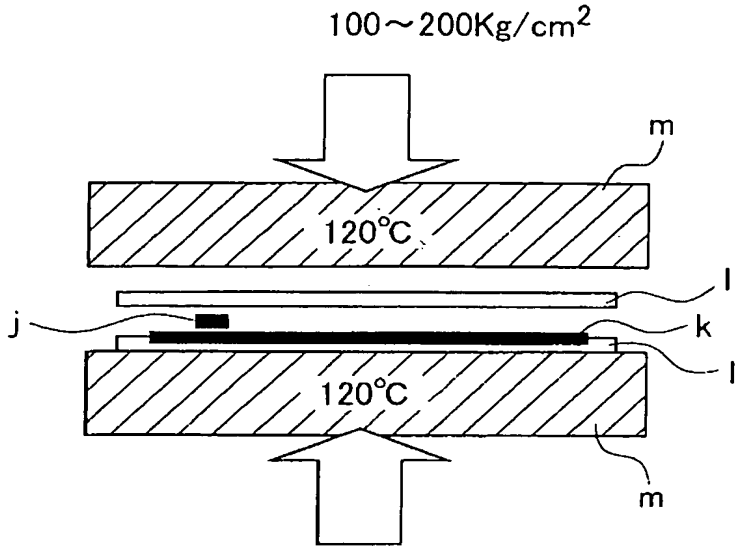


Fig. 20B

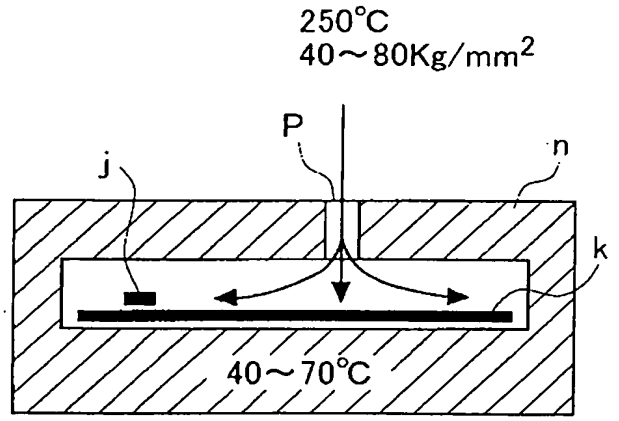


Fig. 21A

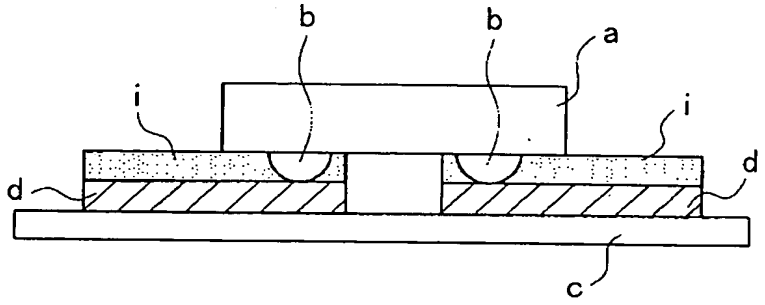


Fig. 21B